EXHIBIT
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ADDING A TRANSFORMER AND OTHER PASSIVE PARTS TO A POWER IC CREATES AN OFF-LINE 3-W SWITCHER THAT FITS IN A WALL PLUG.

OFF-LINE PWM SWITCHING REGULATOR IC HANDLES 3 W

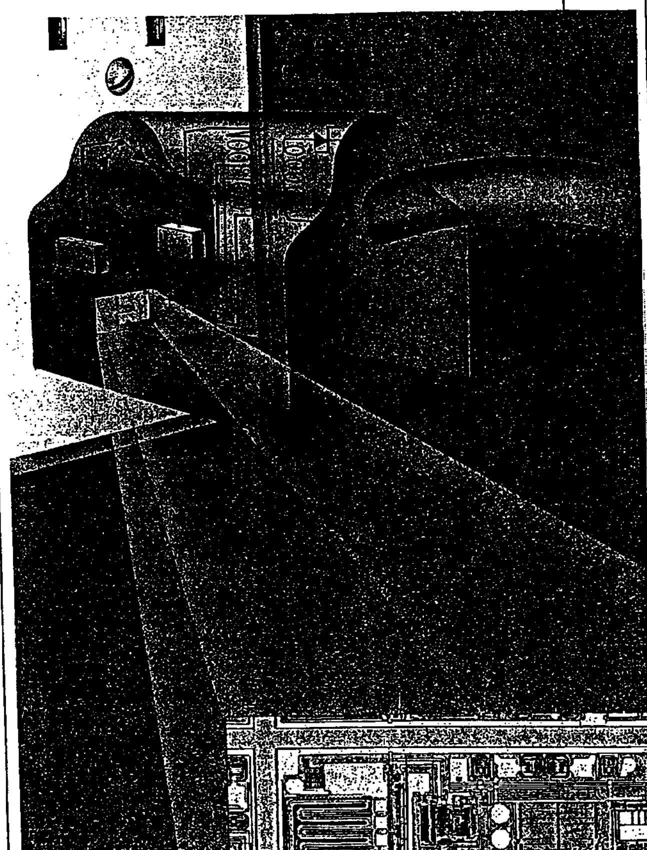
FRANK GOODENOUGH

Now you can operate a battery-powered instrument, computer, modem or other small, low-power electronic device directly from the 115-V ac line without a bulky box to plug in. All that's required is Power Integration's PWR-SMP3 regulator IC to build a 3-W isolated switching power supply. Even if a rectifier bridge and filter are included, the supply's volume can be less than 0.5 in.^{3} *(Fig. 1)*. Typical cost for such a supply in high-volume quantities is between $10 and $20 each, depending on its size and the number built.

The PWR-SMP3 is built on the company's proprietary high-voltage CMOS process. This process puts 5-V logic and small-signal bipolar analog circuits on the same chip.

Housekeeping and/or startup circuits for large off-line supplies represent a typical application for regulators built with the PWR-SMP3. The supply can replace circuits that use bulky 115-V, 60-Hz transformers. It also lends itself to auxiliary outputs in multi-output supplies. In addition, it will simplify the design of multi-output custom circuits.

Other applications for the PWR-SMP3 include remotely located digital panel meters, credit-card readers, and remote, signal-conditioning circuits and modules. Essentially any low-power circuitry where 115 V ac is available can be powered. Because circuit voltage-isolation is a function of the transformer,



not the chip, the PWR-SMP3 can even be used in medical instrumentation or factory-floor automation systems, such as programmable controllers.

Regulators akin to the PWR-SMP3 further the trend to distributed power applications. In such applications, a relatively high voltage (50 to 200 V) is piped around a large multicabinet system to reduce IR line losses. Dc-to-dc

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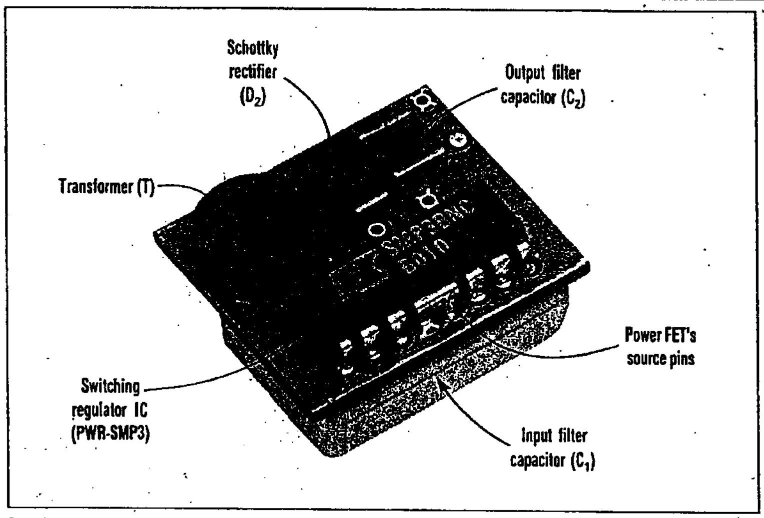


1. OCCUPYING a volume of just one-half cubic inch, this complete off-line switching regulator—built with Power Integrations PWR-SMP3 power IC in a DIP—controls up to 3 W.

converters on each system board reduce the high voltages to typical semiconductor voltage levels *(see* ELECTRONIC DESIGN, *Jan. 11, p. 88).* These regulators can even be smaller because the bridge rectifier and input capacitor aren't needed. With the chip's 3-W rating, supplies could be built to typically deliver 200 mA at 15 V, 250 mA at 12 V, or 600 mA at 5 V. A pair of regulators could thus supply ±15-V power for a slew of op amps. Or one regulator could supply 600 mA of −5.2-V ECL power in a primarily CMOS system.

To construct a complete switching regulator, all that's required are a bridge rectifier and filter, a storage-inductor/isolation transformer, a Schottky diode, several other rectifiers and diodes, and a handful of resistors and capacitors, in addition to the PWR-SMP3 *(Fig. 2)*. Packaged in a 16-pin DIP, the regulator is the supply's heart. Running at 1 MHz to minimize inductor size, the PWR-SMP3's controller section is optimized to implement a voltage-mode flyback circuit. Alternatively, other common pulse-width-modulated (PWM) regulator topologies may also be employed.

The chip's circuit includes all of the blocks needed for a basic PWM regulator and all of the self-protection blocks expected in today's controllers *(Fig. 2, again)*. The input dc voltage (200 V maximum) is applied to the CMOS power FET through the transformer and to a linear preregulator which drops it to the 6-V V_S required to run the control circuits during startup. Once the supply is up and running, the preregulator is turned off. The small-signal circuits on the chip are then powered from the "bootstrap"/feedback output from the transformer through the rectifier-filter formed by diode D_5 and capacitor C_5.

Bypass capacitor C_3 keeps switching noise out of the control circuitry. Diodes D_3 and D_4 snub Ldi/dt transients as the switch turns off. A fast, low-loss Schottky diode—D_2—rectifies the voltage across the isolated output winding of the transformer, which is filtered by C_2 to give 600 mA of regulated 5-V power. Virtually any other voltage can be generated by changing the secondary winding of the transformer.

The basic PWM circuit is conventional. The 0-to-50% duty-cycle pulses from the oscillator turn on the FET switch through the NAND-gate and the FET-gate driver. The sawtooth (ramp) output of the oscillator runs to the PWM comparator which receives its other input from the output of the error amplifier (the output is a function of the difference between the supply's output voltage through the feedback path and the output of the 1.25-V bandgap reference). When the level of the ramp reaches the output of the error amplifier, the comparator flips and turns off the FET switch through the OR gate, PWM latch, NAND gate, and driver.

No Self-Destruct

As noted earlier, the chip is loaded with self-protection features. To start, the FET switch is a sense or mirror, FET with an output that feeds a small fraction of the total drain current through an on-chip current-sensing resistor, R_{sense}. The voltage developed across the resistor is applied to the current-limit comparator. When the drain current exceeds approximately 300 mA, the FET is quickly turned off.

When using this technique, voltage noise can be a problem because typical sense voltages run as low as 200 and 500 mV. Increasing the sense voltage tends to degrade the linear relationship between it and drain current. In this FET, however, proprietary compensation techniques raise the sense voltage while maintaining linearity.

On the input side of the chip, overvoltage and undervoltage (OV/UV) lockout circuits ensure that the input voltage and the 6-V internal (bias) supply are within the required limits before the supply will operate. Input OV lockout is particularly useful in off-line applications where surges or high-energy spikes are apt to be present. The supply shuts down during the transient and starts up when the input returns to the proper range. The OV/UV levels are programmed by the divider formed by resistors R_1 and R_2. Shutdown also occurs when the internal bias voltage is too low for proper circuit operation. Hysteresis in these circuits ensures reliable noise-free operation. The chip can either be shut down or kept from turning on by holding the OV/UV pin low. Turn-on can be delayed—for example, if turn-on of multiple supplies must be sequenced—by hanging a capacitor on the pin.

Typical UV lockout values for

PWR-SMP3 regulator IC are 4.6 V for the trip voltage and 4.8 V for the reset voltage. Input UV turn-off and trip-off voltages are 0.4 and 0.35 V, respectively; input OV trip-off and turn-on voltages are 1.27 and 1.21 V, respectively.

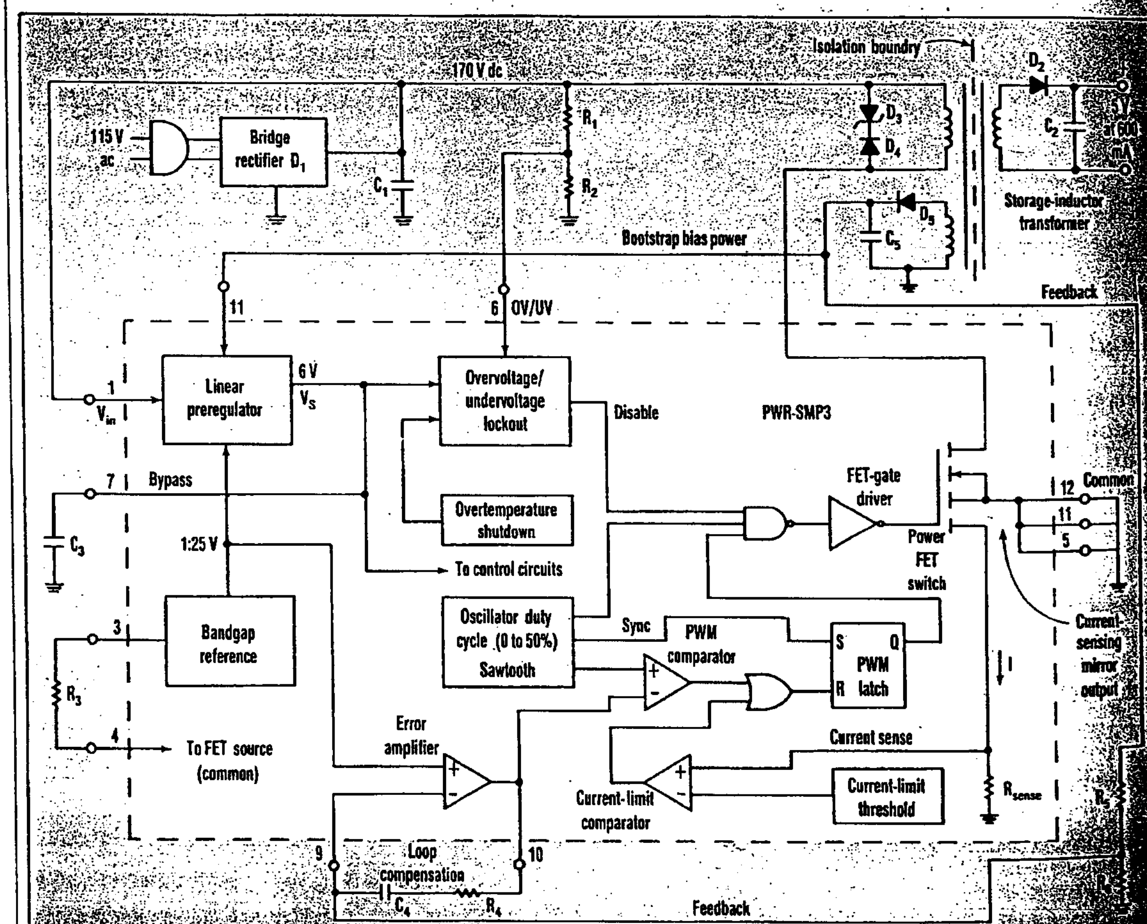
The soft-start circuit consists of a current source and an internal capacitor connected to an intermediate stage of the error amplifier. Until the capacitor is fully charged, the error amplifier output voltage is clamped low, limiting the duty cycle and peak current of the switch during startup. Once the capacitor is fully charged, the amplifier takes over and regulates the output voltage. All shutdown and lockout modes discharge this capacitor, ensuring that the supply always starts from a known state. The over-temperature shutdown circuit turns the switch off when the chip's temperature reaches between 125° and 175°C. Built-in hysteresis makes sure the temperature drops at least 45°C before the switch comes on again.

SUPERIOR CMOS

The chip will operate with input voltages between 36 and 200 V, adapting it to 48-V telecommunications applications. While oscillating at 1 MHz, the chip's quiescent current is just 4 mA. The FET switch's on-resistance is typically 14 Ω, and output capacitance is a low 8 pF. Rise and fall times of the output are typically 40 ns, with an input voltage of 160 V and a drain current of 200 mA.

In its 16-pin, plastic modified bat-wing package, the PWR-SMP3 can operate to 70°C. In the bat-wing package, which is designed to remove heat, the four center pins (4, 5, 12, and 13) are part of the copper lead frame on which the die is mounted. They're tied to the source of the FET and may be used as ground connections. Resistor R_3 is connected between pins 3 and 4 to set the internal operating currents. A separate bond wire connects pin 4 to the chip to minimize the effects of noise on the ground lines.

Power Integrations' process, in which lateral CMOS FETs are used for power switches instead of vertical DMOS FETs, brings more than



2. BY RECTIFYING AND FILTERING the 115-V ac line and applying it to the input of the PWR-SMP3 power IC through a storage-inductor/transformer, and by adding a few parts, a 5-V, 600-mA isolated and regulated PWM switching power supply can be created.

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st low cost to high- and low-voltage silicon power ICs. To start, these devices can be built on virtually any, 5-µm mature CMOS line (similar to many companies, Power Integrations doesn't have a fabrication facility, so it uses multiple foundries). The 400-V FET switches from the process, comparable to so-called logic-level FETs, turn on hard with just 5 V of gate-to-source drive. This reduces gate-drive energy by a factor of four, significantly simplifying drive circuitry (at present, discrete logic-level FETs are limited in voltage rating to about 100 V).

Moreover, Miller capacitance at the switch's gate is usually 1/3 that of similarly rated DMOSFETs, further reducing drive energy and raising switching speeds—which reduces inductor size. Running at 1 MHz, the switch in the PWR-SMP3 takes about 1 mW of drive power, while a typical similarly rated DMOSFET uses about 20 mW.

In addition to easier drive, the positive temperature coefficient of the on- resistance of these high-voltage CMOS power FETs is less than that of similarly rated discrete MOSFETs. At 150°C, the on-resistance of a DMOSFET is 2.5 times its 25°C value, while that of the CMOS IC switch is only twice as great.

The lateral CMOS construction also makes it possible for the package's metal tab to be connected to the source rather than to the switch's drain. This virtually eliminates displacement currents when compared with conventional technology where the drain (or collector) is connected to the case or tab.

These currents flowing through the system chassis and heat sinks contribute to system noise and common-mode electromagnetic-interference-conducted emissions. Lower noise levels may lead to less filtering to meet regulatory agency (FCC, VDE, CSA) requirements. To further increase switching speed, delays in the low-impedance driver were reduced by physically distributing the driver across the area occupied by the power FET itself.□

PRICE AND AVAILABILITY

In a 16-pin plastic DIP, the PWR-SMP3 goes for $6 in lots of 1000. High-volume prices are significantly lower. Small quantities are available from stock.

Power Integrations Inc., 411 Clyde Ave., Mountain View, CA 94043; Art Fury or Doyle Slack, (415) 960-3572. CIRCLE 511

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